Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A stack-gate flash memory array, comprising:
a plurality of transistors, said transistors being arranged in a plurality of rows and a plurality of columns, every two transistors in a same said row being a pair of transistors, one of the source/drain terminals of said pair of transistors being coupled each other, the other source/drain terminal of one of said pair of transistors being coupled to a first bit line, the other source/drain terminal of the other one of said pair of transistors being coupled to a second bit line; and
a plurality of isolated transistors, each said isolated transistor corresponding to one of said pair transistors in a same said row, one of the drain/source terminals of each said isolated transistor being coupled to the drain/source terminal where said pair of transistors is coupled each other, the gate terminal of one of said pair transistor being coupled to a word line, the gate terminal of the other one of said pair transistor being coupled to a word line via the gate terminal of said isolated transistor.

[c2] 2. A stack-gate flash memory array, comprising:
a plurality of rows of transistors, every two transistors in

a same said row being a pair of transistors, one of the source/drain terminals of said pair of transistors being coupled each other, the other source/drain terminal of one of said pair of transistors being coupled to a first bit line, the other source/drain terminal of the other one of said pair of transistors being coupled to a second bit line; and

a plurality of isolated transistors, said isolated transistors being coupled to a common source line, each said isolated transistor corresponding to one of said pair of transistors in a same said row, one of the drain/source terminals of each said isolated transistor being coupled to the drain/source terminal where said pair of transistors is coupled each other, the gate terminal of one of said pair of transistors being coupled to a word line, the gate terminal of the other one of said pair of transistors being coupled to a word line via the gate terminal of said isolated transistor.

[c3] 3. A stack-gate flash memory apparatus, comprising:

a bit line decoder, receiving a bit line signal, for decoding and outputting a bit line selecting signal via one of a plurality of bit lines;

a word line decoder, receiving a word line signal, for decoding and outputting a word line selecting signal via one of a plurality of word lines; and

a stack-gate flash memory array comprising

a plurality of rows of transistors, every two neighbor transistors in a same said row being a pair of transistors, one of the source/drain terminals of said pair of transistors being coupled each other, the other source/drain terminal of one of said of pair of transistors being coupled to a first bit line, the other source/drain terminal of the other one of said pair of transistors being coupled to a second bit line; and

a plurality of isolated transistors, said isolated transistors being coupled to a common source line, each said isolated transistor corresponding to one of said of pair of transistors in a same said row, one of the drain/source terminals of each said isolated transistor being coupled to the drain/source terminal where said pair of transistors is coupled each other, the gate terminal of one of said pair of transistors being coupled to a word line, the gate terminal of the other one of said pair of transistors being coupled to a word line via the gate terminal of said isolated transistor;

wherein said stack-gate flash memory apparatus selects one of said rows according to said bit line selecting signals, and selects one of said isolated transistors and one of the corresponding said pair of transistors, thereby performing the reading and programming operations.